IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

III. Amendments to the Claims.

1. (Currently Amended) A memory controller connected to a semiconductor memory device, comprising:

a clock generating circuit that generates an output clock signal;

a data generating circuit that provides output digital data;

a predetermined number "m" data output terminals that provide output data to the semiconductor memory device in parallel;

m output holding circuits for storing the output digital data synchronously with the output clock signal;

a predetermined number "n" signal output terminals that provide output strobe signals to the semiconductor memory device in synchronism with the output data, where n < m; and

a plurality of output delay circuits including one output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s);

a circuit core region in which the clock generating circuit and data generating circuit are formed; and

an interface region surrounding the circuit core region in which the data output terminals, output holding circuits, signal output terminals, and output delay circuits are formed; wherein

each m output holding circuit is ~~physically~~ adjacent to a corresponding one of the m data output terminals **in a first direction between the corresponding data output terminal and the circuit core region**; and

~~the~~**an** output of each output delay circuit is adjacent to the corresponding p signal output terminal(s) **in the first direction between the corresponding signal output terminal and the circuit core region**.

2. (Currently Amended) The memory controller of claim 1, wherein:

PAGE 4/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

the m output data output terminals and n signal output terminals are ~~linearly~~ aligned with one another **in a second direction**;

the m holding circuits are ~~linearly~~ aligned with one another **in the second direction**; and

the plurality of output delay circuits are ~~linearly~~ aligned with one another **in the second direction** between **the** m holding circuits and the ~~aligned~~ m data output terminals and n signal output terminals.

3. (Original) The memory controller of claim 1, wherein:

the value p is greater than one, and the value n is a multiple of p.

4. (Original) The memory controller of claim 1, wherein:

value of p is selected from the group consisting of one and two.

5. (Original) The memory controller of claim 1, wherein:

the value of p is one.

6. (Original) The memory controller of claim 1, wherein:

the value of p is two; and

each of the plurality of output delay circuits has an output terminal arranged equidistant from the corresponding two signal output terminals.

7. (Previously Presented) The memory controller of claim 1, further including:

a plurality of data input terminals that receive input data from the semiconductor memory device;

a signal input terminal for every "q" data input terminals, where "q" is an integer greater than 2, each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data;

PAGE 5/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

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an input delay circuit corresponding to each signal input terminal that delays a received device input clock from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal, ~~the~~**each** input delay circuit~~s being arranged between the~~ **having a circuit input position that is aligned with the corresponding** signal input terminal~~s~~ **in the first direction** and **a circuit output position that is offset in the second direction with respect to the corresponding signal input terminal**~~positions where the input delay circuits output the input strobe signals~~; and

an input holding circuit corresponding to each data input terminal, each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit; wherein

the input data is transmitted to the data generating circuit through the data input terminals.

8. (Currently Amended) The memory controller of claim 1, further including:

a plurality of data input terminals that receive input data from the semiconductor memory device;

a signal input terminal for every "q" data input terminals, where "q" is an integer greater than 2, each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the input data;

an input delay circuit corresponding to each signal input terminal that delays a received device input clock signal from the semiconductor memory device by a predetermined amount to generate an input strobe signal, the input delay circuits being arranged between the signal input terminals and positions where the input delay circuits output the input strobe signals; and

an input holding circuit corresponding to each data input terminal, each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit;

PAGE 6/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

a first wiring corresponding to each data input terminal that transmits digital data to a corresponding input holding circuit; and

a second wiring corresponding to each input holding circuit that transmits the input strobe signal from a corresponding input delay circuit to the input holding circuit; wherein

the first and second wiring corresponding to each input holding circuit being ~~essentially~~ equal in length.

9. (Original) The memory controller of claim 1, wherein:

the m data output terminals are also data input terminals that receive input data from the semiconductor memory device in parallel; and

the n signal output terminals are also signal input terminals for receiving device input clock signals from the semiconductor memory device in synchronism with the input data.

10. (Original) The memory controller of claim 1, wherein:

the output holding circuits transmit output digital data synchronously with both a rising edge and a falling edge of the output clock signal.

11. (Currently Amended) The memory controller of claim 1, further including:

a plurality of data input terminals that receive input data from the semiconductor memory device;

a signal input terminal for every "q" data input terminals, where "q" is an integer greater than 2, each signal input terminal receiving an device input clock signal from the semiconductor memory device in synchronism with the input data; and

an input delay circuit corresponding to each signal input terminal that delays a received device input clock form the semiconductor memory device signal by a predetermined amount to generate an input strobe signal, ~~the~~**each** input delay circuits ~~being arranged between the~~ **having a circuit input**

PAGE 7/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

position that is aligned with the corresponding signal input terminals **in the first direction** and **a circuit output position that is offset in the second direction with respect to the corresponding signal input terminal**~~positions where the input delay circuits output the input strobe signals~~;

an input holding circuit corresponding to each data input terminal, each group of q input holding circuits holding input data in synchronism with the input strobe signal from a corresponding input delay circuit; wherein

the input holding circuits transmit input data to the data generating circuit synchronously with both a rising edge and a falling edge of the corresponding input strobe signal.

12. (Original) The memory controller of claim 1, further including:

the semiconductor memory device being coupled to the memory controller by the m data output terminals and the n signal output terminals.

13. **(Currently Amended)** The memory controller of claim 1, further including:

~~a circuit core region in which the clock generating circuit and data generating circuit are formed; and~~

~~an interface region surrounding the circuit core region in which the data output terminals, output holding circuits, signal output terminals, and output delay circuits are formed; wherein~~

each output holding circuit comprising a first latch circuit.

14. **(Currently Amended)** The memory controller of claim 13, further including:

the data output terminals are data input/output (I/O) terminals;

the signal output terminals are signal I/O terminals;

m input holding circuits corresponding to the data I/O terminals formed in the interface region, each input holding circuit comprising a second latch circuit connected to a corresponding data I/O terminal by a first wiring,

PAGE 8/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

the input holding circuits holding input data in synchronism with a corresponding input strobe signal; and

an input delay circuit connected to each signal I/O terminal by a second wiring, each input delay circuit delaying a received device input clock from the semiconductor memory device signal by a predetermined amount to generate an input strobe signal, each input strobe signal being connected to a corresponding second latch circuit by a third wiring; wherein

the length of the first wiring to each second latch circuit is ~~essentially~~ equal to the sum of the lengths of the second and third wirings corresponding to the same second latch circuit.

15. (Currently Amended) A memory controller connected to a semiconductor memory device, comprising:

a predetermined number "m" data input terminals that receive input data from the semiconductor memory device;

a predetermined number "n" signal input terminals, each signal input terminal receiving a device input clock signal from the semiconductor memory device in synchronism with the input data, where m > n;

a data storing circuit for receiving digital data from the data input terminals;

n input delay circuits that delay received device input clock signals from the semiconductor memory device by a predetermined amount to generate input strobe signals;

m input holding circuits that hold the input data in synchronism with the input strobe signals generated by the input delay circuits; and

m data input wirings, each data input wiring transmitting an input data value from one data input terminal to a corresponding input holding circuit; and

m signal input wirings transmitting one input strobe signal from one input delay circuit to a corresponding input holding circuit; wherein

PAGE 9/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

the data input wiring and signal input wiring for the same corresponding input holding circuit being ~~essentially~~ equal in length.

16. (Original) The memory controller of claim 15, wherein:

the input delay circuits are arranged between the signal input terminals and locations where the input delay circuits output the input strobe signals.

17. (Original) The memory controller of claim 15, wherein:

the input holding circuits transmit input data to the data generating circuit synchronously with both a rising edge and a falling edge of the corresponding input strobe signal.

18. (Original) The memory controller of claim 15, further including:

the semiconductor memory device being coupled to the memory controller by the m data input terminals and the n signal input terminals.

19. (Original) The memory controller of claim 15, further including:

a circuit core region in which the data storing circuit are formed; and

an interface region surrounding the circuit core region in which the data input terminals, input holding circuits, signal input terminals, input delay circuits, signal input wirings, and data input wirings are formed; wherein

each input holding circuit comprising a first latch circuit.

20. (Currently Amended) The memory controller of claim 15, further including:

the m data input terminals and n signal input terminals are ~~linearly~~ aligned with one another **in a first direction**; and

the m input holding circuits are ~~linearly~~ aligned with one another **in the first direction** parallel to the data input terminals and signal input terminals.

21. (Original) The memory controller of claim 15, further including:

PAGE 10/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42

a clock generating circuit that generates an output clock signal;

a data generating circuit that provides output digital data;

a plurality of data output terminals that that provide output data to the semiconductor memory device in parallel;

a signal output terminal for every "q" data output terminals, where "q" is an integer greater than 2, each signal output terminal providing an output strobe signal to the semiconductor memory device in synchronism with the output data;

an output delay circuit for every "p" signal output terminal(s), where p is an integer greater than zero, each output delay circuit delaying the output clock signal by a predetermined amount to transmit an output strobe signal to the corresponding p signal output terminal(s); and

an output holding circuit corresponding to each data output terminal, each group of q output holding circuits holding output data in synchronism with the output strobe signal from the corresponding output delay circuit.

PAGE 11/19 * RCVD AT 11/13/2006 4:29:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-3/22 * DNIS:2738300 * CSID:14089770174 * DURATION (mm-ss):05-42